EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

2. Authorization for this examiner's amendment was given in a telephone interview with Laura C. Brutman on 10/27/2008.

3. The following claims had been amended:

Claim 1 -12: (Canceled).

Claim 13: A time-sliced processor for use in a communication system comprising:

a master control unit including a time slot table and a partial sum table for any time slot granularity;

a data cache configured to receive input data and to cache intermediate data at chip or sub-chip resolution; and

a plurality of signal processing elements, each element comprising:

a cache configured to receive data from the data cache and to cache intermediate data at chip or sub-chip resolution,

a data selector connected to an output of the cache,

a symbol computing engine connected to an output of the data selector, and

a symbol integrator connected to an output of the symbol computing engine

wherein the master control unit is configured to allocate the partial sum table on a per signal processing element basis to extend signal processing control flexibility across time slots, and

wherein the communication system is a spread-spectrum communication system.

Claim 14 -15: (Canceled).

Claim 16: The time-sliced processor of claim 13, wherein the time-sliced processor is independent of a communication protocol.

Claim 17: (Canceled).

Claim 18: The time-sliced processor of claim 13, wherein the time-sliced processor supports multiple spread spectrum applications that run at different granularities when optimized.

Claim 19: The time-sliced processor of claim 13, wherein the signal processing elements are finger processing elements.

Claim 20: The time-sliced processor of claim 13, wherein the symbol computing engine is a despreader.

Claim 21: The time-sliced processor of claim 13, wherein the master control unit is configured to configure and control the data cache and the signal processing elements.

Claim 22: The time-sliced processor of claim 13, wherein the master control unit is configured to schedule time-sliced signal processing in the data cache and the signal processing elements.

Claim 23: The time-sliced processor of claim 13, wherein the master control unit is configured to allocate time slots, maintain synchronization of the signal processing elements, and maximize throughput.

Claim 24: (Canceled).

Claim 25: The time-sliced processor of claim 13, wherein the master control unit is linked to an external processing element to manage time slot allocation among the signal processing elements.

Claim 26: The time-sliced processor of claim 13, wherein the time-sliced processor is configured to call programming across different protocols in a given application space.

Claim 27: The time-sliced processor of claim 13, wherein the time-sliced processor is configured to perform speed grading of components.

Claim 28: A master control unit in a time-sliced processor of a communication system having a data cache, which receives input data and caches intermediate data, and a plurality of signal processing elements, the master control unit comprising:

a time slot table; and

a partial sum table; and

a plurality of signal processing elements, each element comprising:

a cache configured to receive data from the data cache and to cache intermediate data at chip or sub-chip resolution,

a data selector connected to an output of the cache,

a symbol computing engine connected to an output of the data selector, and

a symbol integrator connected to an output of the symbol computing engine, wherein the master control unit is configured to configure and control the data cache and the signal processing elements for any time slot granularity, and to control the data cache to cache at chip or sub-chip resolution, and to schedule time-sliced signal processing in the data cache and the signal processing elements.

Claim 29: (Canceled).

Claim 30: The master control unit of claim 28, wherein the master control unit is configured to allocate time slots, maintain synchronization of the signal processing elements, and maximize throughput.

Claim 31: The master control unit of claim 28, wherein the master control unit is configured to allocate the partial sum table on a per searcher basis to extend search control flexibility across time slots.

Claim 32: The master control unit of claim 28, wherein the master control unit is linked to an external processing element to manage time slot allocation among the signal processing elements.

Claim 33: The master control unit of claim 28, wherein the communication system is a spread-spectrum communication system.

Claim 34: The master control unit of claim 22, wherein master control unit is configured to enable the time-sliced processor to support multiple spread spectrum applications that run at different granularities when optimized.

Claim 35: The master control unit of claim 28, wherein the master control unit is configured to enable the time-sliced processor to call programming across different protocols in a given application space.

Claim 36: The master control unit of claim 28, wherein the master control unit is configured to enable the time-sliced processor to perform speed grading of components.

Claim 37: A time-sliced processor for use in a communication system comprising:

a data cache for receiving input data and for caching intermediate data at chip or sub-chip resolution;

a plurality of signal processing means, each signal processing means comprising:

a cache for receiving data from the data cache and for caching intermediate data at chip or sub-chip resolution,

a data selecting means connected to an output of the cache,

a symbol computing means connected to an output of the data selecting means, and

a symbol integration means connected to an output of the symbol computing means; and

a master control means, including a time slot table and a partial sum table, for configuring and controlling the data cache and the signal processing means for any time slot granularity,

wherein the partial sum table is configured to complete a signal processing function across multiple time slots.

Claim 38: The time-sliced processor of claim 13, wherein the partial sum table is configured to complete a signal processing function across multiple time slots.

Claim 39: The time-sliced processor of claim 13, wherein the data cache is configured to cache intermediate data for completing a signal processing function across multiple time slots.

Claim 40: The master control unit of claim 28, wherein the partial sum table is configured to complete a signal processing function across multiple time slots.

Claim 41: The master control unit of claim 28, wherein the master control unit is configured to allocate the partial sum table on a per signal processing element basis to extend signal processing control flexibility across time slots.

Claim 42: The time-sliced processor of claim 13, wherein the time slot granularity is at chip boundary.

Claim 43: The time-sliced processor of claim 13, wherein the time slot granularity is at sub-chip boundary.

Claim 44: The master control unit of claim 28, wherein the time slot granularity is at chip boundary.

Claim 45: The master control unit of claim 28, wherein the time slot granularity is at sub-chip boundary.

Claim 46: The time-sliced processor of claim 37, wherein the time slot granularity is at chip boundary.

Claim 47: The time-sliced processor of claim 37, wherein the time slot granularity is at sub-chip boundary.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to ABDULLAH AL KAWSAR whose telephone number is (571)270-3169. The examiner can normally be reached on 7:30am to 5:00pm, EST.

5. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng Ai T. An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

6. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Meng-Ai An/
Supervisory Patent Examiner, Art Unit 2195

/Abdullah-Al Kawsar/
Examiner, Art Unit 2195